CLAIMS

1. A level shift circuit comprising:

first and second P-channel transistors of which sources are connected to a high-voltage power supply; and

first and second N-channel transistors of which sources are grounded,

wherein complementary input signals in phase with and in opposite phase to an input signal from a low power-supply voltage operating circuit are respectively inputted to gates of the first and second N-channel transistors,

a drain of the first N-channel transistor is connected to a drain of the first P-channel transistor and a gate of the second P-channel transistor,

a drain of the second N-channel transistor is connected to a drain of the second P-channel transistor and a gate of the first P-channel transistor,

the level shift circuit further comprises a resistance connecting the drain of the first N-channel transistor with the drain of the second N-channel transistor, and

the drain of the second N-channel transistor serves as an output terminal to a high power-supply voltage operating circuit.

2. The level shift circuit of Claim 1,

wherein the resistance is constructed of a P-channel transistor, and

the P-channel transistor is grounded at its gate, connected to the drain of the first N-channel transistor at its source, and connected to the drain of the second N-channel transistor at its drain, to be in the normally ON state.

3. The level shift circuit of Claim 1,

wherein the resistance is constructed of an N-channel transistor, and

the N-channel transistor is connected to a high-voltage power supply at its gate, connected to the drain of the first N-channel transistor at its source, and connected to the drain of the second N-channel transistor at its drain, to be in the normally ON state.

4. The level shift circuit of Claim 1,

wherein the resistance is constructed of a P-channel transistor, and

the P-channel transistor receives an ON/OFF operation switch signal at its gate, connected to the drain of the first N-channel transistor at its source, and connected to the drain of the second N-channel transistor at its drain.

5. The level shift circuit of Claim 1,

wherein the resistance is constructed of an N-channel transistor, and

the N-channel transistor receives an ON/OFF operation switch signal at its gate, connected to the drain of the first N-channel transistor at its source, and connected to the drain of the second N-channel transistor at its drain.

6. The level shift circuit of Claim 4 or 5,

wherein the ON/OFF operation switch signal is an operation mode switch signal received from outside.

7. The level shift circuit of any one of Claims 1 to 6,

wherein the drains of the first and second N-channel transistors serve as differential output terminals for the high power-supply voltage operating circuit.

8. A semiconductor integrated circuit comprising the level shift circuit of any one of

Claims 1 to 7.